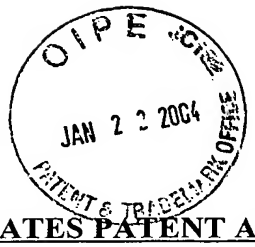
DOCKET NO. 8229-017-27 CIP



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Jim HUNTER, et al. ART UNIT: 2872
SERIAL NO.: 10/-29,875 EXAMINER: Alessandro V. Amari
FILING DATE: December 31, 2001
FOR: HIGH CONTRAST GRATING LIGHT VALVE

DECLARATION, 37 C.F.R. §1.608(b)

ASSISTANT COMMISSIONER FOR PATENTS
PO BOX 1450
ALEXANDRIA, VA 22313-1450

SIR:

We, James Hunter, Chris Gudeman, David Amm and Akira Tomita, do hereby declare and state that:

1. We are the co-inventors of the U.S. Patent Application Serial Nos. 10/029,875, filed December 31, 2001 and 10/050,994, filed January 22, 2002.

2. At the time the inventions claimed in U.S. Patent Application Serial Nos. 10/029,875 and 10/050,994 were made, we were employees of Silicon Light Machine, a division of Cypress Semiconductor Corporation. As conditions incident to employment, we assigned the entire right, title and interest in and to these inventions, and these applications, to Cypress Semiconductor Corporation.

3. The four of us, well prior to December 18, 1998, conceived of and developed a grating light valve comprised of a substrate, typically formed of silicon, and a dielectric layer formed on the substrate, such as silicon dioxide. The invention conceived of and reduced to practice in advance of December 18, 1998 further included a conductive trace formed in the dielectric layer, intended to allow charges trapped at the dielectric layer to escape. The provision of the

conductive trace was particularly focused on trapped charges present on the surface of the dielectric layer. The reflective light processing element we conceived of and reduced to practice before December 18, 1998 further included a plurality of ribbons formed above the substrate and the conductive trace.

4. We have reviewed the claims of the above-captioned patent application, and although we are not patent attorneys, as we best understand them, they correspond to the subject matter we invented prior to December 18, 1998.

5. As evidence of our prior invention, attached hereto is Exhibit A which is a summary of the invention. The date on this summary has been redacted, we understand, but we confirm that the original document, which this is a copy of, reflects a date well in advance of December 18, 1998. The summary accurately describes the subject matter claimed in the above-captioned patent application. This summary was prepared by the four of us.

6. This summary, and the processing steps needed to prepare the necessary device, were addressed and reflected in an invention notebook maintained at Silicon Light Machine ("SLM") a division of Cypress Semiconductor Corporation, and are reflected here to in Exhibit B, which includes pages 29-33 of that invention notebook. The date of those entries is in advance of December 18, 1998.

7. At or about the same time, and in any event, in advance of December 18, 1998, cross-sectional representations of the device prepared were made. These cross-section representations, including the contact trace, are included as Exhibit C.

8. In order to provide a conductive trace on the dielectric layer, to allow trapped charges to escape, it was necessary to develop a new etching process. Two of us, James Hunter and David Amm, developed that process while traveling via airplane to the Texas facility of Cypress Semiconductor Corporation well in advance of December 18, 1998. The process we developed is

reflected in drawings prepared during that trip, which are attached hereto as Exhibit D.

9. Subsequent to the preparation of the grating light valve 6.0 prototype described above, but prior to December 18, 1998, schematics reflecting the grating light valve were prepared. Corresponding schematics are presented as Exhibit E, without date. As shown, the zero order grating light valve has a conductive trace connection that runs through the dielectric layer, to allow the escape of trapped charges. Pictured are the substrate, two sets of ribbons, and gaps in between. The physical structure is reflected in the third schematic. The conductive trace goes from substrate contact to ribbon post, as illustrated.

10. Accordingly, in light of the contemporaneous documents submitted herewith, we confirm that the subject matter of the claims of the above-captioned patent application as recited above, had been conceived of by us, and reduced to practice, in advance of December 18, 1998.

All statements made herein of own knowledge are true, and all statements made on information and belief are believed true. Further, we are aware that willful false statements and the like are punishable by fine, imprisonment, or both, 18 U.S.C. §1001, and that such willful false statements may jeopardize the validity of the above-captioned patent application, and any patent to issue thereon.

Dated: 7 JAN 2004

JAMES HUNTER

Dated: 7 JAN 2004

CHRIS GUDEMAN

Dated: Jan 8/04

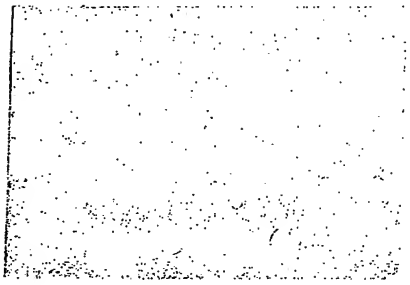
DAVID AMM

Dated: Jan 22, '04

Akira Tomita

AKIRA TOMITA

EXHIBIT A



GLV 6.0

Summary

The purpose of the GLV 6.0 mask set is to test the feasibility of zero order with a GLV style device (ribbons and gaps of roughly equal widths). This device was not meant to be sealed. There are four mask steps, Via1 (contact from gap Al to substrate), Ribbon, Post, and Thick Al. The mask set has been designed for the CIS Ultratech stepper and the die size and layout is compatible with the Rover package. The number of test structures has been kept to a minimum for rapid layout. There are no test modules; all testable structures are in the main array. There are 11 superpixels, consisting of 60 25.5 um pixels each. The superpixels are electrically isolated. There are a limited number of other test structures, designed to test contact resistances and gap and ribbon reflectivity. The contact resistance test structures are intended to be bondable to the Rover package.

Main Array

Superpixel #	Name	Length (um)	Width (um)	Redundancy	Layout name
1	DCP1	200	4.375	3	xTestDCP1L200
2	DCM3	200	3.875	3	xTestDCM3L200
3	DCM2	200	4.000	3	xTestDCM2L200
4	DCM1	200	4.125	3	xTestDCM1L200
5	DC0	200	4.250	3	xTestDC0L200
6	DCP1	200	4.375	3	xTestDCP1L200
7	DCP2	200	4.500	3	xTestDCP2L200
8	DCP3	200	4.625	3	xTestDCP3L200
9	L300	300	4.375	1, centered	xTestDCP1L300
9		150	4.375	2, edges	
10	L500	500	4.375	1, centered	xTestDCP1L500
10		50		2, edges	
11	DCP1	200	4.375	3	xTestDCP1L200

Substrate Contact

4 contact pads are located around the array.

Test Structures

Reflectivity

Ribbon Reflectivity

Gap Reflectivity

Contact Resistance

2 bondable pads with 10 vias

2 bondable pads with 1 via

These 4 structures are arranged in a line so that 4-point substrate resistance measurements may be made.

Proposal for Short Loop for Zero Order:

- abandon the standard sealing approach
- use hand assembled Rovers for on-the-wall display testing
- 4 mask layers:
  - post
  - Ribbon
  - M2 – thick Al
  - Via – gap contact
- field mask (thin metal)

Process:

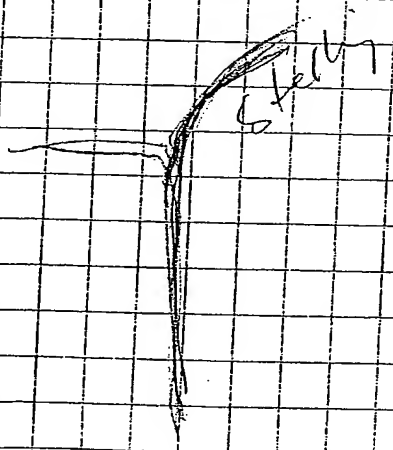
- Silicon wafer start
- oxide/SiN 400Å
- Sac poly deposition 8500Å
- Post mask
- Sac poly etch
- SiN ribbon deposition
- Ribbon photo
- SiN ribbon etch through to sac poly and substrate(ie ribbon and etch stop)
- M2 deposition 3kÅ Al sp
- M2 photo
- M2 etch
- Sac poly partial etch with undercut – SF6 or XeF2?
- Via photo
- Via etch
- Thin Al deposition (evap?) 500Å
- contact anneal?

EXHIBIT B

PROS

could use
type 10% AC
could easily
get substitute
content

- order a
piece of cake
at your moms
work on STS

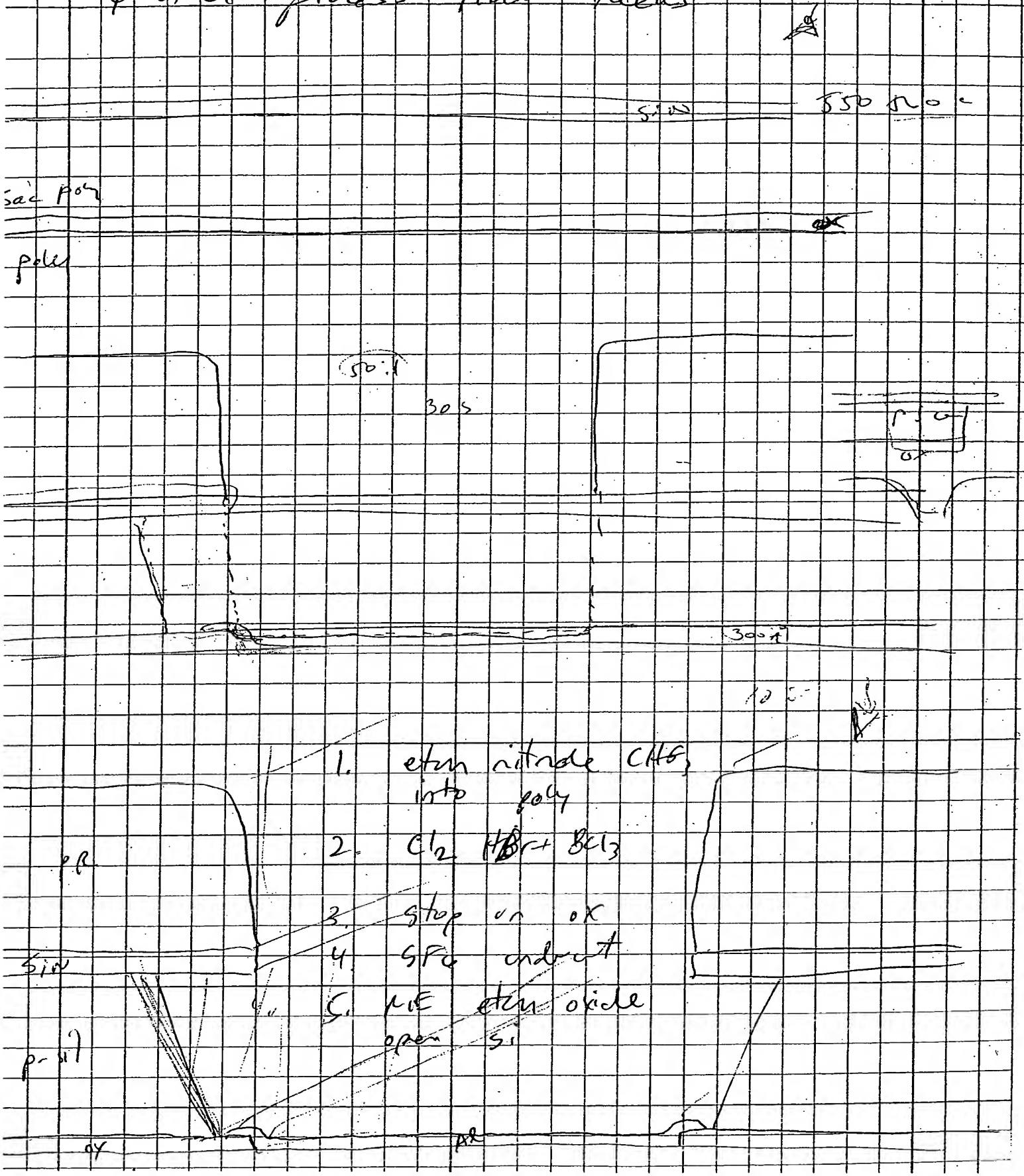


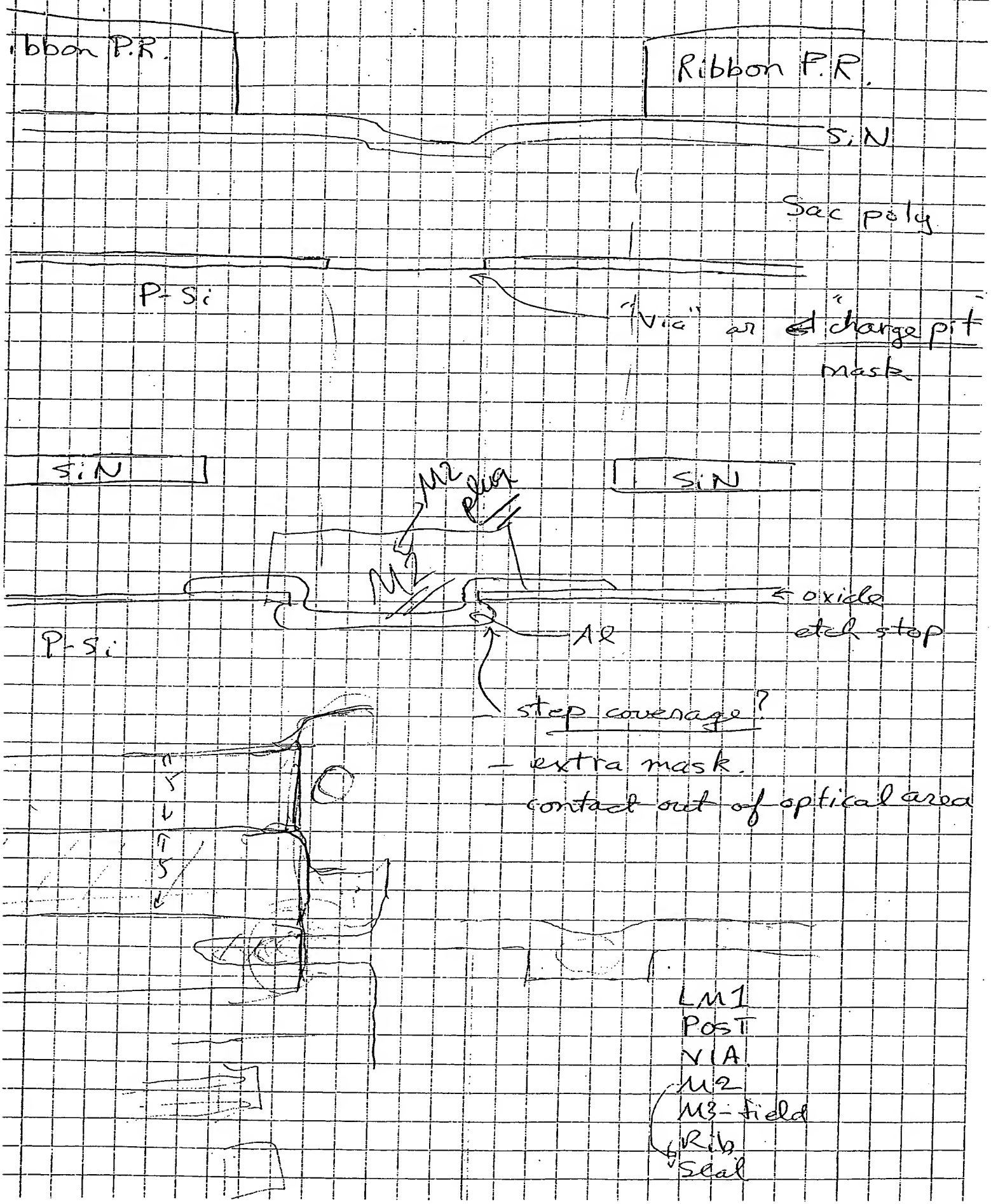
CONS

- need to
figure out
fat %

7/29

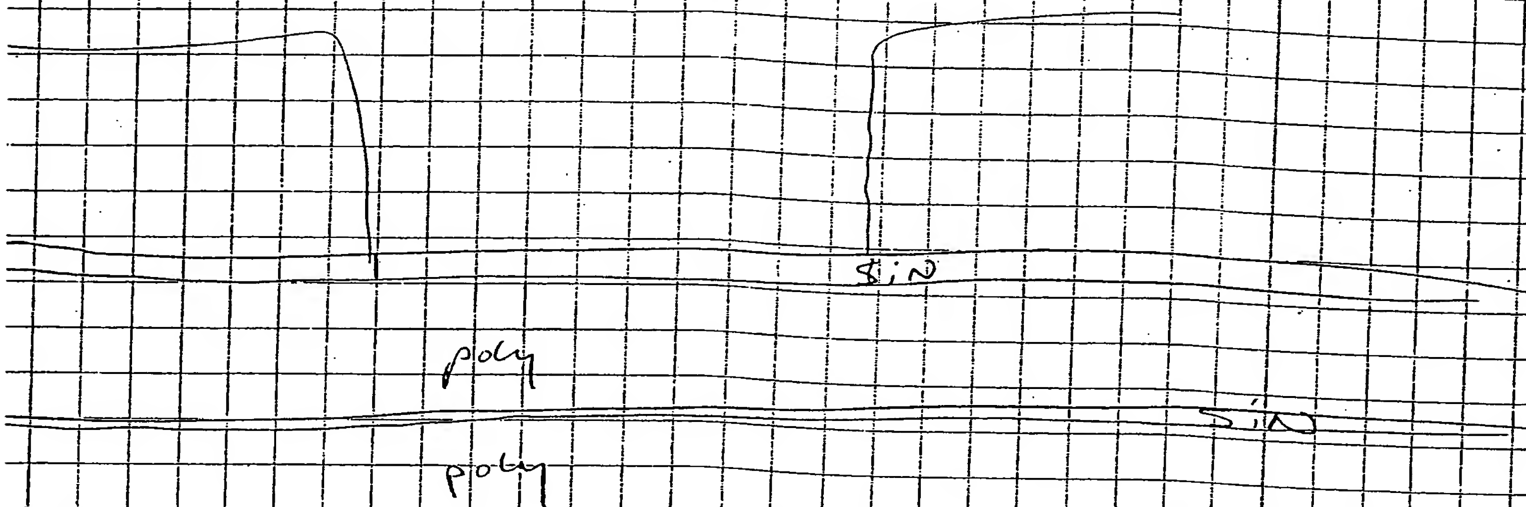
ϕ order process flow ideas




Ribbon P.R.
Ribbon P.R.
Si N
Sac poly
P- Si
"Via" or "Change pit" mask
Si N
Si N
M2
Plug
M2
oxide
etch stop
Al
P- Si
step coverage?
- extra mask.
- contact out of optical area
LM1
POST
VIA
M2
M3 - field
Rib
Seal

O. wider design

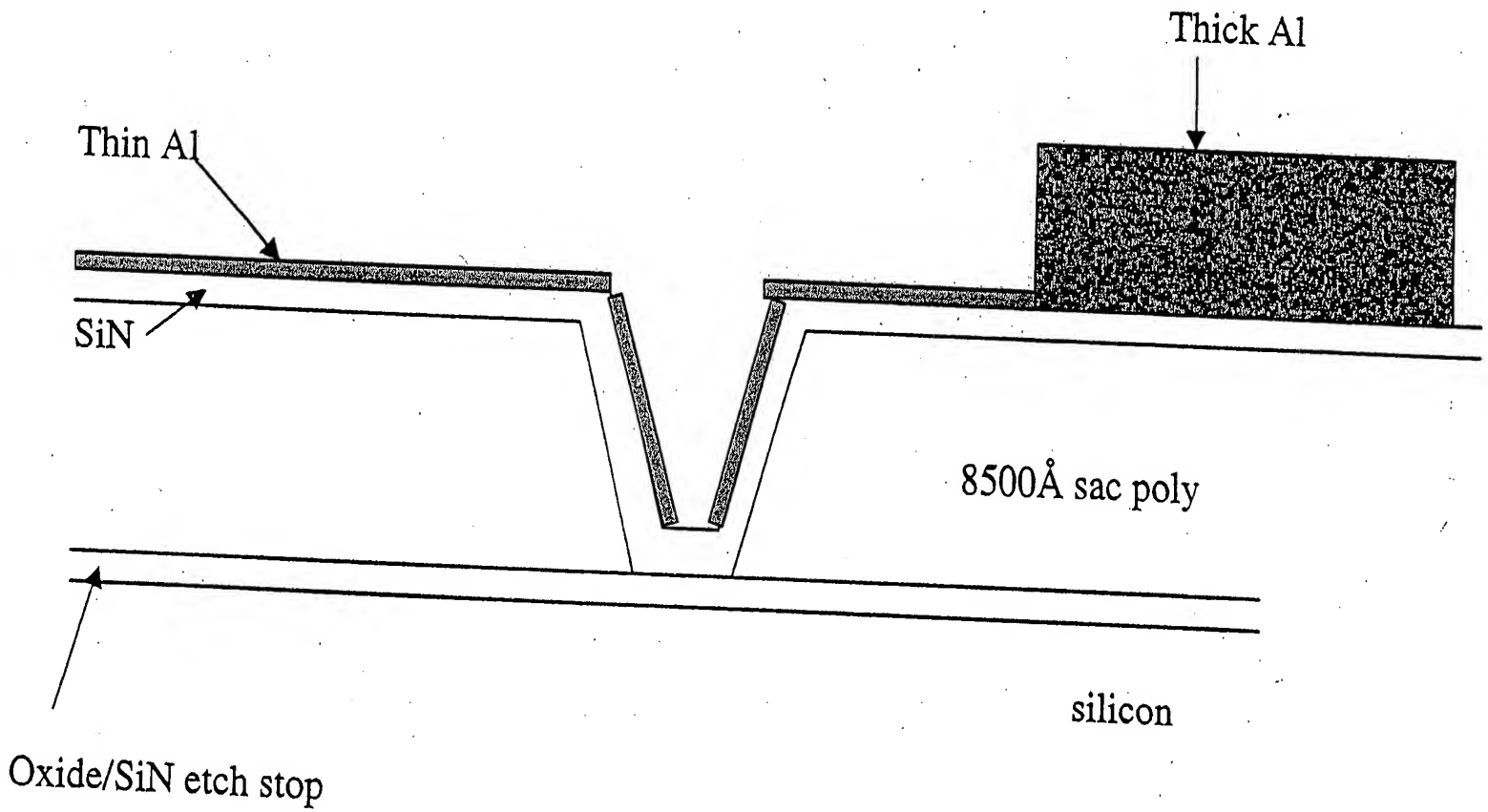
processing identical (just prior to thin metal dep)



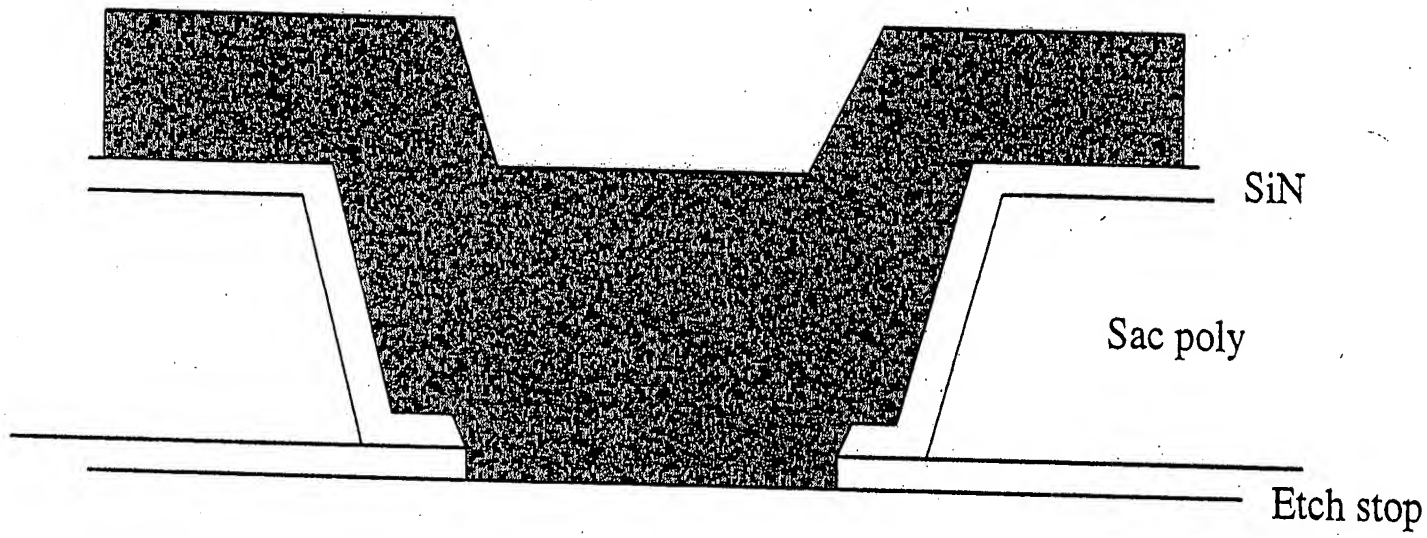
ribbon mask + etch
short release
maybe add via mask + etch
at overlap

EXHIBIT C

Active post:


Thick Al
Thin Al
SiN
8500Å sac poly
silicon
Oxide/SiN etch stop

Substrate contact



Gap contact

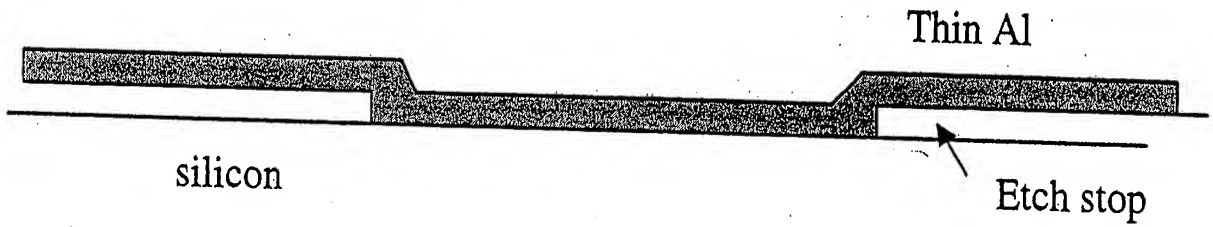


EXHIBIT D

(1)

8600 Å - 0 Å
+ 300 Å

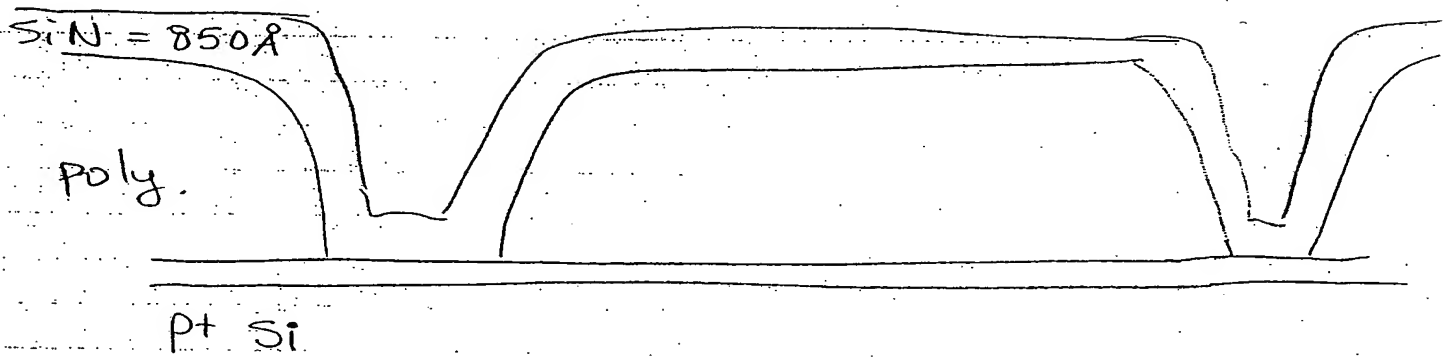
sac poly.

tch stop = thermal oxide 500 Å

P^+ Si Substrate

Post Mask - etch poly, stop on oxide

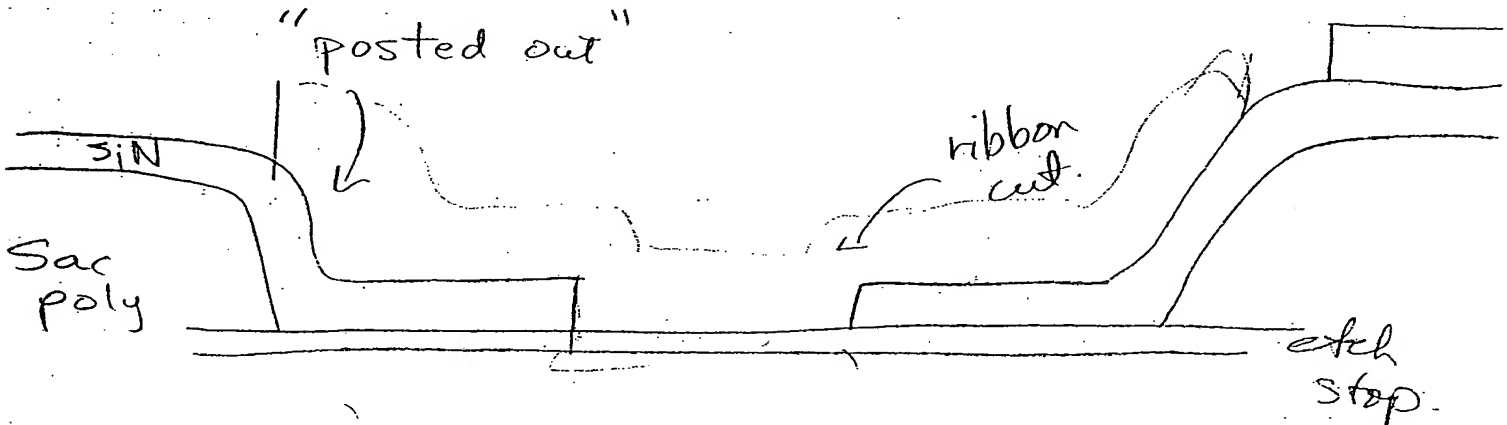
dep. ribbon = 850 Å



Ribbon Photo and Etch.

↳ continue etch through.
500Å oxide etch stop.

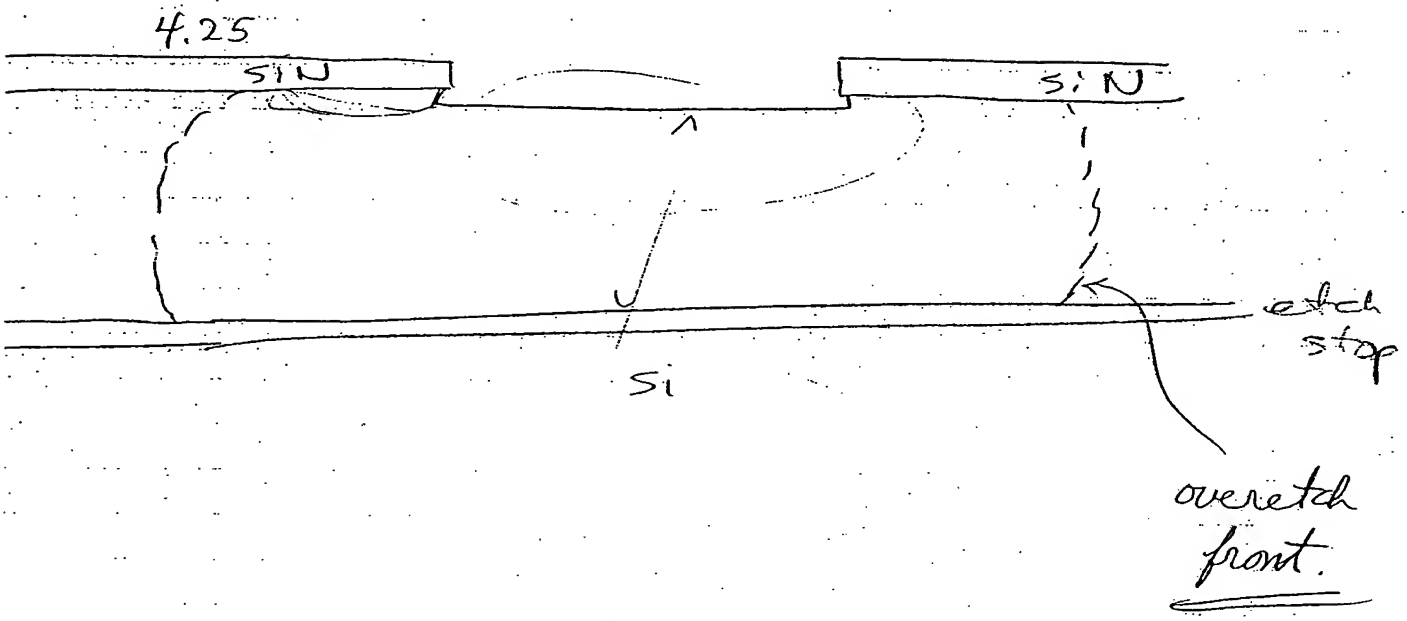
substrate contact.



After Etch - standard, agressive resist strip to clear polymer.

M2 layer before partial release.
After ribbon etch + strip resist.

- partial XeF_2 release → 2x to 1.5x overetch.

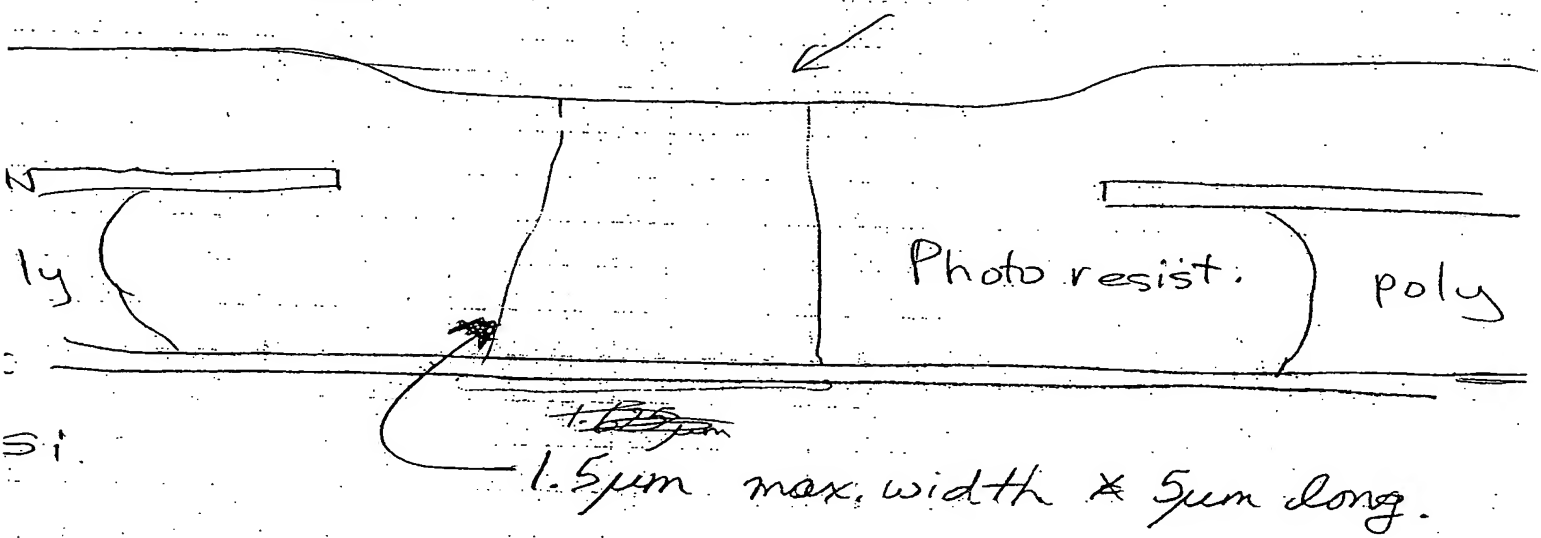


M2 ~~dep~~ dep – sputter Al pure – 3000 Å

M2 photoetch.

Resist Dep.

Via Photo.



Oxide etch 500Å; into Silicon substrate.

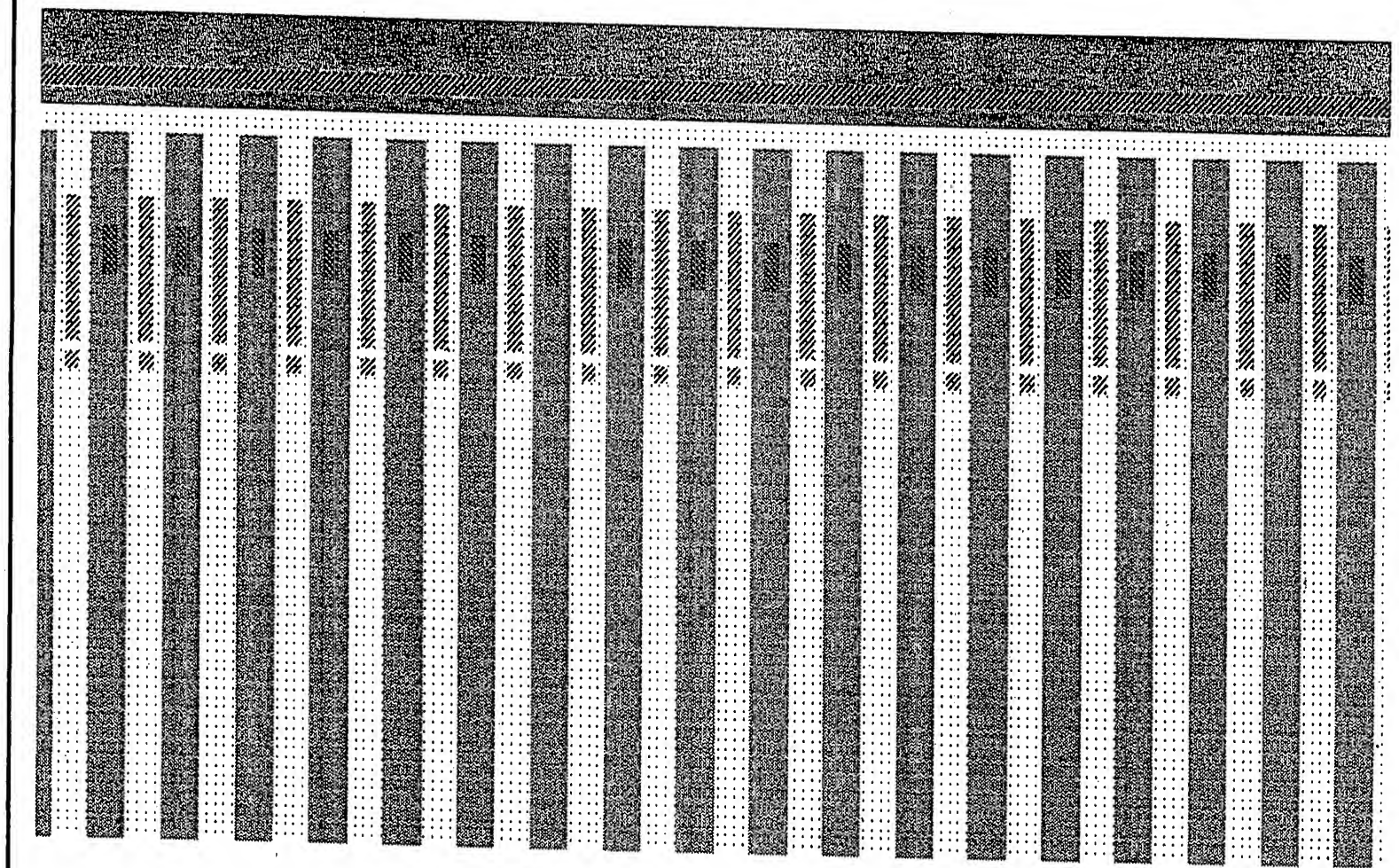
Thin Al evap = 500 Å

contact Anneal.

- "loosely" spaced die on wafer stepping.

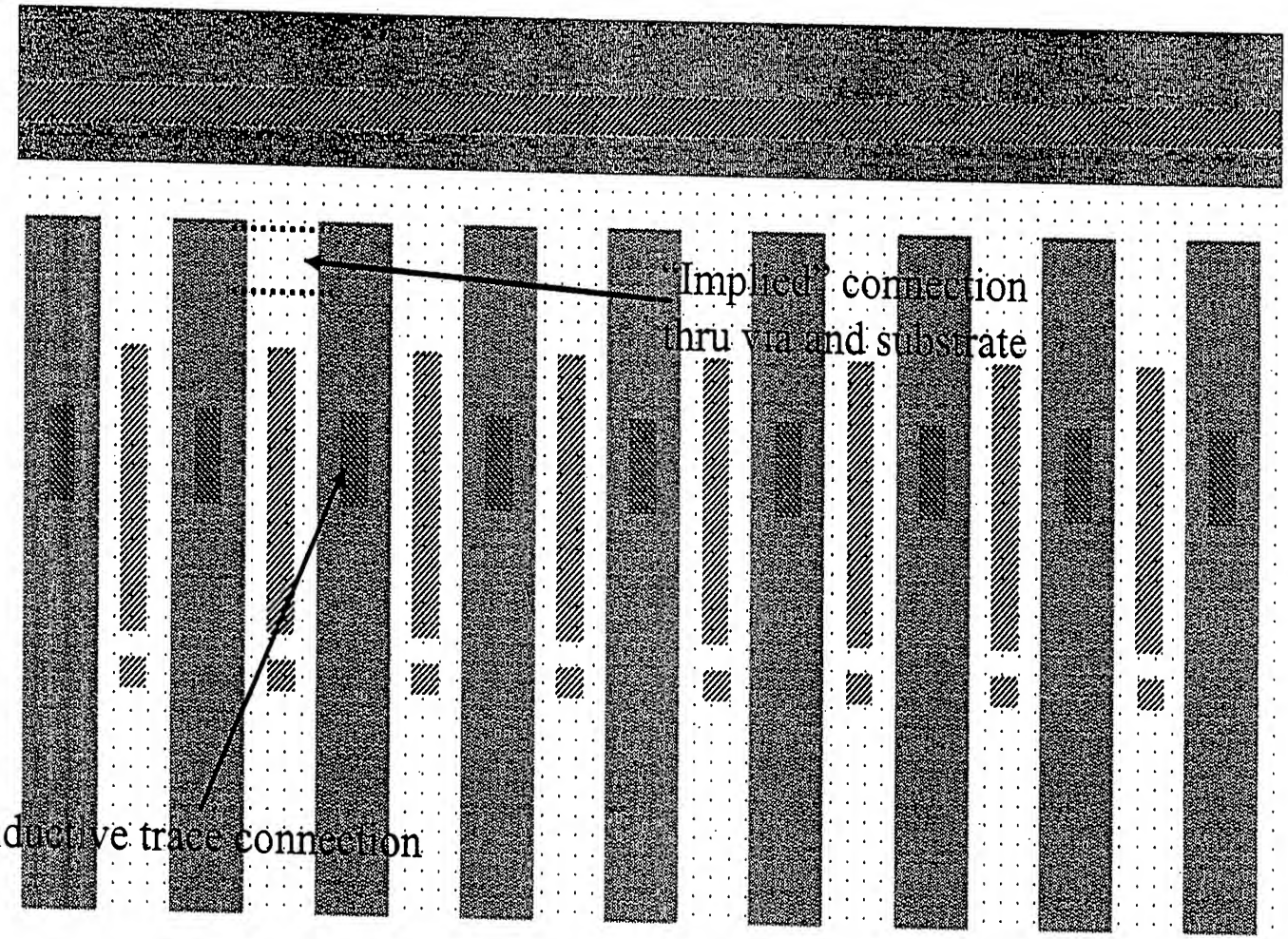
EXHIBIT E

0-Order Layout

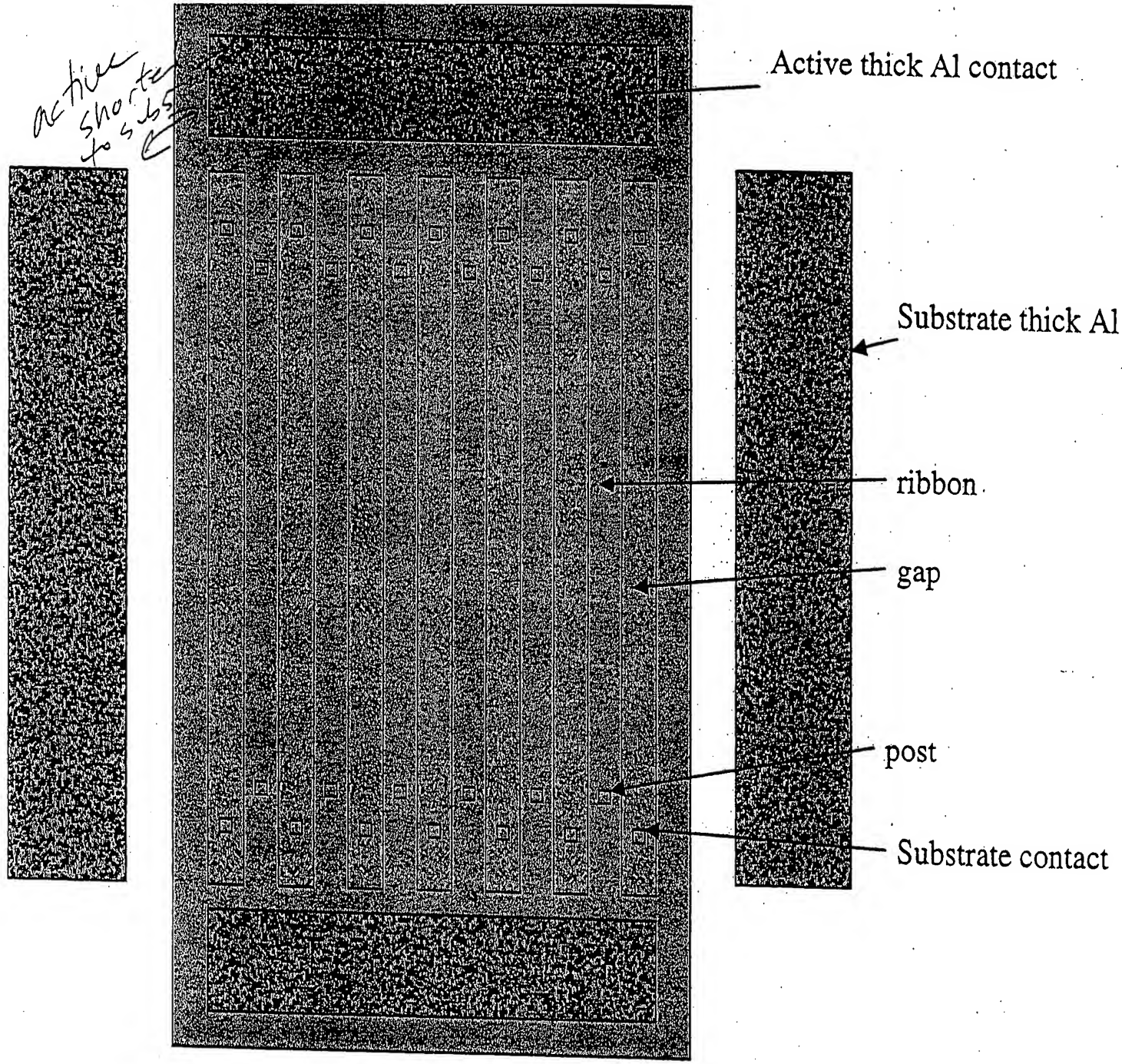


SILICON LIGHT MACHINES

0-Order Layout – charge structure close up



SILICON LIGHT MACHINES


Active thick Al contact
Substrate thick Al
ribbon
gap
post
Substrate contact